

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended): In a color projection-type television display having
2 digital convergence correction data, a method for producing a convergence correction signal
3 comprising:
4 reading out convergence correction data stored in a memory;
5 supplying said convergence correction data to a first circuit operable to produce
6 an analog signal from said convergence correction data; and
7 producing said convergence correction signal based on said analog signal,
8 wherein a data rate at which said convergence correction data is supplied to said
9 first circuit varies when said television display displays a high definition video signal which has
10 a blanking period shorter than that of a NTSC signal.

1 2. (Original): The method of claim 1 wherein said reading out said
2 convergence correction data is performed with a varying data rate so that said convergence
3 correction data is supplied to said first circuit at a varying data rate.

1 3. (Original): The method of claim 1 wherein said reading out said
2 convergence correction data includes producing addresses to access said memory, said addresses
3 being produced at a varying rate so that said convergence correction data is supplied to said first
4 circuit at a varying data rate.

1 4. (Original): The method of claim 1 wherein a memory location spacing
2 between said convergence correction data which correspond to an edge region of a display range
3 of a horizontal scan line is less than a memory location spacing between convergence correction
4 data corresponding to a central portion of said display range.

1 5. (Original): The method of claim 1 wherein said producing is a step of
2 filtering said analog signal with a low-pass filter component to produce said convergence
3 correction signal, said filtering including altering at least one filter parameter value of said low-
4 pass filter component.

1 6. (Original): The method of claim 5 wherein altering at least one filter
2 parameter value of said low-pass filter component is dependent on locations on said display
3 corresponding to said convergence correction data.

1 7. (Currently amended): A color projection-type display system having a
2 convergence correction signal generation component comprising:
3 an analog signal generator for producing said convergence correction signal, said
4 analog signal generator having an input portion for receiving digital convergence correction data;
5 and
6 a memory coupled to supply digital data to said analog signal generator,
7 said memory configured with convergence correction data, said convergence
8 correction data comprising first data corresponding to correction points along a horizontal scan
9 line,
10 said correction points being unevenly distributed along said horizontal scan line,
11 wherein correction points proximate an edge portion of said horizontal scan line have smaller
12 separation than corrections points in a central portion of said horizontal scan line, so that the rate
13 at which said convergence correction data is received by said analog signal generator varies
14 when said television display displays a high definition video signal which has a blanking period
15 shorter than that of a NTSC signal.

1 8. (Original): The convergence correction signal component of claim 7
2 wherein said analog signal generator includes a low-pass filter for producing said convergence
3 correction signal and a filter parameter selection circuit for selectively adjusting a parameter of
4 said low-pass filter depending on said convergence correction data.

1 9. (Currently amended): A color projection-type television system including
2 a convergence correction signal generating apparatus for correcting convergence in a display
3 area of said television system, said convergence correction signal generating apparatus
4 comprising:

5 a memory configured with convergence correction data;

6 an address generation circuit operatively coupled to said memory to access said
7 convergence correction data; and

8 an analog signal generation circuit coupled to said memory to receive said
9 convergence correction data from said memory and operable to produce said convergence
10 correction signal from said convergence correction data,

11 said convergence correction data corresponding to correction points along a
12 horizontal scan line, wherein separation between correction points located in a central portion of
13 said display area is greater than separation between correction points located in an edge portion
14 of said display area, wherein the rate at which said convergence correction data is received by
15 said address generation circuit varies when said television display displays a high definition
16 video signal which has a blanking period shorter than that of a NTSC signal.

1 10. (Original): The apparatus of claim 9 wherein said convergence correction
2 data is stored in said memory such that a first pair of adjacent convergence correction data is
3 separated by zero or more empty memory locations and a second pair of adjacent convergence
4 correction data is separated by zero or more empty memory locations, said first pair of adjacent
5 convergence correction data have a memory location spacing different from said second pair of
6 adjacent convergence correction data.

1 11. (Currently amended): A color projection-type television display including
2 a convergence correction signal generating apparatus for correcting convergence in a display
3 area of said display, said convergence correction signal generating apparatus comprising:
4 a memory configured with convergence correction data;
5 an address generation circuit operatively coupled to said memory to access said
6 convergence correction data; and
7 an analog signal generation circuit coupled to said memory to receive said
8 convergence correction data from said memory and operable to produce convergence correction
9 signals from said convergence correction data,
10 said convergence correction data being stored in said memory in ordered fashion
11 corresponding to a horizontal scanning order,
12 wherein when said television display displays a high definition video signal which
13 has a blanking period shorter than that of a NTSC signal, then said convergence correction data
14 being stored in said memory such that a first pair of adjacent convergence correction data is
15 separated by zero or more empty memory locations and a second pair of adjacent convergence
16 correction data is separated by zero or more empty memory locations, said first pair of adjacent
17 convergence correction data have a memory location spacing different from said second pair of
18 adjacent convergence correction data.

1 12. (Original): The apparatus of claim 11 wherein pairs of adjacent
2 convergence correction data have smaller separation for those convergence correction data
3 corresponding to an edge portion of said display area than for those convergence correction data
4 corresponding to a central portion of said display area.

1 13. (Original): The apparatus of claim 11 wherein said analog signal
2 generation circuit includes a low pass filter component, said low pass filter component having at
3 least one filter parameter value selectable from among a plurality of filter parameter values, said
4 filter parameter value being selected based on locations of said display area corresponding to
5 said convergence correction data received by said analog signal generation circuit.

1 14. (Original): The apparatus of claim 13 wherein said at least one filter
2 parameter value is a time constant of said low pass filter component.

1 15. (Original): The color projection-type television display of claim 11 as
2 incorporated in a color projection-type television system.

1 16. (Currently amended): A display device for use in a color projection-type
2 television, a convergence correction signal generating apparatus for correcting convergence in a
3 display area of said display device comprising:
4 a memory configured with convergence correction data;
5 an address generation circuit operatively coupled to said memory to access said
6 convergence correction data; and
7 an analog signal generation circuit coupled to receive said convergence correction
8 data from said memory and operable to generate convergence correction signals based on said
9 convergence correction data,
10 said address generation circuit configured to generate an address at a variable rate
11 so that said analog signal generation circuit receives said convergence correction data at a data
12 rate that varies when said television display displays a high definition video signal which has a
13 blanking period shorter than that of a NTSC signal.

1 17. (Original): The apparatus of claim 16 wherein said rate of address
2 generation is higher for convergence correction data corresponding to an edge region of a display
3 of said projection-type television than for convergence correction data corresponding to a center
4 region of said display.

1 18. (Original): The apparatus of claim 16 wherein said analog signal
2 generation circuit includes a low pass filter component, said low pass filter component having at
3 least one filter parameter value selectable from among a plurality of filter parameter values.

1 19. (Original): The apparatus of claim 18 wherein said at least one filter
2 parameter value is a time constant of said low pass filter component.

1 20. (Original): The apparatus of claim 18 wherein one of said filter parameter
2 values is selected based on locations of said display area corresponding to said convergence
3 correction data received by said analog signal generation circuit.

1 21. (Original): The apparatus of claim 16 wherein said analog signal
2 generation circuit comprises:
3 a digital-to-analog converter configured to receive said convergence correction
4 data to produce a first analog signal;
5 a low-pass filter circuit coupled to said digital-to-analog converter to produce a
6 second analog signal from said first analog signal;
7 current amplifier circuit coupled to said low-pass filter to produce a third analog
8 signal from said second analog signal; and
9 a convergence yoke coupled to said current amplifier to receive said third analog
10 signal to control scanning of an electron beam in accordance with said third analog signal.

1 22. (Currently amended): A color projection-type television comprising:
2 a color display apparatus;
3 circuitry having an input to receive a television signal and having an output
4 coupled to deliver a video signal to said color display apparatus, said video signal produced from
5 said television signal; and
6 a convergence correction signal generating apparatus having an output to deliver
7 convergence correction signals to said color display apparatus to correct convergence in a
8 display area of said color display,
9 said convergence correction signal generating apparatus comprising:
10 a memory configured with convergence correction data;
11 an address generation circuit operatively coupled to said memory to access
12 said convergence correction data; and
13 an analog signal generation circuit coupled to receive said convergence
14 correction data from said memory and operable to generate said convergence correction signals
15 based on said convergence correction data,
16 said address generation circuit configured to generate an address at a
17 variable rate so that said analog signal generation circuit receives said convergence correction
18 data at a data rate that varies when said television display displays a high definition video signal
19 which has a blanking period shorter than that of a NTSC signal.

1 23. (Original): The color projection-type television of claim 22 wherein said
2 circuitry includes a tuner portion for receiving said television signal and a video processing
3 portion for producing said video signal from said television signal.

1 24. (Currently amended): A convergence correction circuit adapted for use in
2 a color display device, said convergence correction circuit producing a convergence correction
3 signal to correct convergence on a display area of said color display device, said convergence
4 correction circuit comprising:

5 first means for generating a convergence correction signal based on digital data;
6 second means for storing a plurality of digital convergence correction data, said
7 second means operatively coupled to said first means to supply said plurality of digital
8 convergence correction data to said first means; and

9 third means operatively coupled to said second means for outputting said plurality
10 of digital convergence correction data from said second means at a variable data rate when said
11 television display displays a high definition video signal which has a blanking period shorter
12 than that of a NTSC signal, wherein said first means is supplied with said digital convergence
13 data at said variable data rate.

1 25. (Original): The circuit of claim 24 wherein first means includes means for
2 filtering an analog signal and means for varying a filter parameter value of said means for
3 filtering based on locations of said display area corresponding to said digital convergence
4 correction data supplied to said first means.

1 26. (Original): The circuit of claim 24 wherein some of said digital
2 convergence correction data is stored in non-contiguous storage locations in said second means,
3 so that adjacent digital convergence correction data have memory location spacings of zero or
4 more empty storage locations.

1 27. (Original): The circuit of claim 24 wherein said third means includes
2 means for generating storage location information, wherein said storage location information is
3 supplied to said second means to output said digital convergence correction data, said storage
4 location information being generated at a varying rate so that said digital convergence correction
5 data is outputted at a variable data rate.